What is claimed is:

1. An array-type processor in which a multiplicity of processor elements, which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, are arranged in rows and columns; and in which said instruction codes of this multiplicity of processor elements are successively switched by a state control unit in accordance with a computer program that has been installed in advance and said event data; wherein:

said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary; and

said array-type processor includes an event distributing means for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation.

2. An array-type processor according to claim 1, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units.

3. An array-type processor according to claim 1, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units.

4. An array-type processor according to claim 1, wherein:

data buses for transmitting processing data of said plurality of processor elements are arranged in matrix form;

a plurality of switch elements, which switch-control a wiring

configuration of said data buses in accordance with instruction codes that are individually set as data, are arranged in matrix form together with said processor elements;

said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements; and

said event distributing means is constituted by said data buses that are switch-controlled by said switch elements.

5. An array-type processor according to claim 2, wherein all of said plurality of state control units are interconnected by said event distributing means.

6. An array-type processor according to claim 2, wherein:

said plurality of state control units are arranged in rows and columns; and

said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity.

7. An array-type processor according to claim 6, wherein:

said plurality of state control units are arranged in rows and columns, and

said state control units are connected by said event distributing means to state control units that are located in eight directions in the vicinity.

8. An array-type processor according to claim 6, wherein:

said plurality of state control units are arranged in rows and columns;

and

said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions.

9. An array-type processor according to claim 1, wherein:

a central control unit is provided for distributing said event data to said plurality of state control units; and

said central control unit is connected by said event distributing means to all of said plurality of state control units.

10. An array-type processor according to claim 6, wherein:

a central control unit is provided for distributing said event data to said plurality of state control units; and

said central control unit is connected by said event distributing means to all of said plurality of state control units.

11. An array-type processor according to claim 1, wherein: an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

12. An array-type processor according to claim 6, wherein: an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

13. An array-type processor according to claim 11, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means.

14. An array-type processor according to claim 11, wherein output selection means is provided for each of said state control units, said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means.

15. An array-type processor according to claim 1, wherein:

said multiplicity of processor elements is divided into element areas that correspond in number to said state control units;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

16. An array-type processor according to claim 6, wherein:

said multiplicity of processor elements is divided into element areas that correspond in number to said state control units;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are

supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

17. An array-type processor according to claim 11, wherein:

said multiplicity of processor elements is divided into element areas that correspond in number to said state control units;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.